REMARKS

Claims 1-37 remain pending in the present application. In the Office Action, claims 1-9, 11-19, 21, 23-25, 27-34, and 36-37 were rejected under 35 U.S.C. § 102(b) as allegedly being anticipated by Maruyama (U.S. Patent No. 6,052,763). The Examiner's rejections are respectfully traversed.

With regard to independent claims 1, 11-13, 23, and 32, Applicants describe and claim a memory management unit for managing a memory storing data arranged within a plurality of memory pages. The claimed memory management unit includes a security check unit coupled to receive a physical address generated during execution of a current instruction. The physical address resides within a selected memory page and the security check unit is configured to use the physical address to access at least one security attribute data structure located in the memory to obtain a security attribute of the selected memory page. The security check unit is also configured to compare information conveyed by a security attribute of the current instruction to information conveyed by the security attribute of the selected memory page and to produce an output signal dependent upon a result of the comparison. The memory management unit is configured to access the selected memory page dependent upon the output signal.

Maruyama is directed to a memory unit and a method for coordinating atomic memory transactions in a tightly coupled multiprocessor system. Maruyama describes a system bus 15 and a system bus interface 16 coupled to a decoder 21, a register 22, a comparator 23, and a master ID table 24. See Maruyama, Figure 4. The system bus 15 and the system bus interface 16 provide an access address to the decoder 21, which identifies whether the access address is for a conventional address space or for an atomic address space in a DRAM 19. See Maruyama, col. 6, ll. 11-15. The system bus 15 and the system bus interface 16 also provide a bus master ID to the

register 22, the comparator 23, and the master ID table 24. See Maruyama, col. 6, ll. 44-47. In an atomic transaction mode, an ID of the bus master that is making the atomic transaction request is temporally stored in the register 22. Subsequently, the comparator 23 compares the temporally stored bus master ID with the ID of the requesting device. See Maruyama, col. 7, ll. 26-34. The master ID table 24 uses the provided bus master ID to distinguish whether or not a bus master is a processor. See Maruyama, col. 6, ll. 47-50.

On page 2 of the Office Action, the Examiner alleges that the system bus interface unit 16 uses an access address to determine a bus master ID. Applicants respectfully disagree. As discussed above, the system bus interface unit 16 provides the access address to the decoder 21 and the bus master ID to the register 22. As discussed above, the access address is used to determine whether the referenced portion of the DRAM 19 is a conventional address space or an atomic address space. The provided bus master ID identifies the last bus master to have memory access rights. See Maruyama, col. 6, ll. 33-34. However, Maruyama does not teach or suggest that the bus master ID is determined using the access address. Furthermore, the bus master ID table 24 is not located in the DRAM 19, so it does not appear that the access address can be used to access the bus master ID table 24. Thus, Maruyama does not teach or suggest using the physical address to access at least one security attribute data structure located in the memory to obtain a security attribute of the selected memory page, as set forth in independent claims 1, 11-13, 23, and 32.

On page 2 of the Office Action, the Examiner also alleges that the comparator 23 compares values from the master ID table 24 to the bus master ID. The Examiner admits on page 3 of the Office Action that the comparator 23 does not *directly* compare values from the master ID table 24 to the bus master ID. Instead, the Examiner alleges that the comparator 23 *indirectly*

compares values from the master ID table 24 to the bus master ID because the information stored in the register 22 comes from the bus master ID table 24. Applicants respectfully disagree and submit that the register 22 does not receive the stored bus master ID from the bus master ID table 24. In contrast, as discussed above, the system bus 15 and the system bus interface 16 provide the bus master ID to the register 22, the comparator 23, and the master ID table 24. See Maruyama, col. 6, ll. 44-47.

Thus, Applicants respectfully submit that Maruyama fails to teach or suggest a security check unit configured to compare information conveyed by a security attribute of the current instruction to information conveyed by the security attribute of the selected memory page, as set forth in independent claims 1, 11-13, 23, and 32. Consequently, Maruyama also fails to teach or suggest producing an output signal dependent upon a result of the comparison, or accessing the selected memory page dependent upon the output signal.

For at least the aforementioned reasons, Applicants respectfully submit that independent claims 1, 11-13, 23, 32, and all claims depending therefrom are not anticipated by Maruyama and request that the Examiner's rejections of these claims under 35 U.S.C. 102(b) be withdrawn.

In the Office Action, claims 10, 20, 22, 26, and 35 were rejected under 35 U.S.C. § 103(a) as allegedly being unpatentable over Maruyama in view of Applicants' admitted prior art. The Examiner's rejections are respectfully traversed.

To establish a *prima facie* case of obviousness, the prior art reference (or references when combined) must teach or suggest all the claim limitations. *In re Royka*, 490 F.2d 981, 180 U.S.P.Q. 580 (CCPA 1974). Claims 10, 20, 22, 26, and 35 depend from independent claims 1, 13, 23, and 32. As discussed above, Maruyama fails to teach or suggest many aspects of the present invention set forth in independent claims 1, 13, 23, and 32. The Examiner relies on the

admitted prior art to teach use of a user/supervisor bit and/or a read/write bit. However, Applicants respectfully submit that the admitted prior art does not remedy the aforementioned deficiencies of the primary reference. Thus, Applicants respectfully submit that claims 10, 20, 22, 26, and 35 are not obvious over Maruyama in view of the admitted prior art and request that the Examiner's rejections of these claims under 35 U.S.C. 103(a) be withdrawn.

For the aforementioned reasons, it is respectfully submitted that all claims pending in the present application are in condition for allowance. The Examiner is invited to contact the undersigned at (713) 934-4052 with any questions, comments or suggestions relating to the referenced patent application.

Respectfully submitted,

Date: 7/19/04

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